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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,352	10/31/2003	Zhiwei Xu	5589-05001	2525

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,352	XU ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-8,10,13-15 and 17-20* is/are rejected.

7)☒ Claim(s) *3-4, 9, 11, 12, and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 13, 2005 have been fully considered but they are not persuasive [see Conclusion for further details].

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 5, 8, 10, 13-15 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Verkuil et al (6202029).

Regarding claim 1, Verkuil et al disclose [see Fig. 1] a method for determining a surface voltage of an insulating film (oxide 12), wherein a wafer (wafer 15) comprises the insulating film (12) formed on a substrate (substrate 14), the method comprising: depositing [via corona gun 18] a charge on an upper surface of the insulating film (12) [see also Abstract]; measuring [apparatus 10] a current to the wafer (15) during said depositing; and determining [Kelvin probe 20] the surface voltage of the insulating film (12) from the current [see col. 3, lines 15-43].

Regarding claim 2, Verkuil et al disclose said determining [via Kelvin probe 20] comprises determining [via controller 32] an accumulated voltage as a function of the current, wherein the function is determined by calibration of a charge deposition system used for said

depositing, and determining [via controller 32] the surface voltage from the accumulated voltage and a reference voltage of said depositing.

Regarding claim 5, Verkuil et al disclose said depositing [via corona gun 18] comprises depositing the charge over time [see Abstract], the method further comprising determining [via SPV 34] charge build up on the upper surface by integrating the current over the time [see Abstract].

Regarding claim 8, Verkuil et al disclose altering [via controller 32] a control voltage (voltage supply 30) after said measuring [via apparatus 10] and repeating said depositing [via corona gun 18], said measuring [via apparatus 10], and said determining [via Kelvin probe 20].

Regarding claim 10, Verkuil et al disclose determining [via apparatus 10] a parameter representing an electrical property of the insulating film (12) from the surface voltage.

Regarding claim 13, Verkuil et al disclose performing the method during a semiconductor fabrication process [see col. 1, lines 14-16].

Regarding claim 14, Verkuil et al disclose a method, comprising: measuring [via apparatus 10] a first current to a wafer (wafer 15) during deposition of a first charge on a surface of the wafer (15), wherein the wafer (15) comprises an insulating film (oxide 12) formed on a Substrate (substrate 14); determining [via Kelvin probe 20] a first surface voltage of the insulating film (12) from the first current; measuring [via apparatus 10] a second current to the wafer (15) after a high current mode deposition [via SPV tool 34] of a second charge on the surface of the wafer (15); and determining [via Kelvin probe 20] a second surface voltage of the insulating film (12) from the second current, wherein the first and second surface voltages are determined at approximately the same location on the insulating film (12).

Regarding claim 15, Verkuil et al disclose repeating said measuring [via apparatus 10] the second current and said determining [via Kelvin probe 20] the second surface voltage until a Q-V sweep is measured.

Regarding claim 17, Verkuil et al disclose the first charge and the second charge are deposited with the same charge deposition system [corona gun 18].

Regarding claim 18, Verkuil et al disclose the first charge and the second charge are deposited with different charge deposition systems.

Regarding claim 19, Verkuil et al disclose a method for determining charge vs. voltage data for an insulating film (oxide 12), wherein a wafer (wafer 15) comprises the insulating film (12) formed on a substrate (substrate 14), the method comprising: depositing [via corona gun 18] a charge on an upper surface of the insulating film (12); altering [via controller 32] a control voltage (via voltage supply 30) during said depositing such that a current to the wafer (15) is substantially constant over time; and determining [Kelvin probe 20] a voltage of the insulating film (12) as a function of the charge deposited on the insulating film (12), wherein the voltage is determined from the control voltage and the current, and wherein the charge deposited on the insulating film (12) is determined from the current and the time.

Regarding claim 20, Verkuil et al disclose the control voltage is a reference voltage of the charge deposition system [corona gun 18] or a reference voltage of the wafer (15).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verkuil et al (6202029) in view of IBM (IBM Technical Disclosure Bulletin, Vol. 32, Vol. 9A, 1990, pp. 14-17).

Regarding claim 6, Verkuil et al disclose [see Fig. 1] a method for determining a surface voltage of an insulating film (oxide 12) comprising: depositing [via corona gun 18] a charge on an upper surface of the insulating film (12) [see also Abstract]; measuring [apparatus 10] a current to the wafer (15) during said depositing; and determining [Kelvin probe 20] the surface voltage of the insulating film (12) from the current. However, they do not disclose illuminating an upper surface of an insulating film and determining a band-bending voltage as claimed. IBM disclose depositing [via charging bias 11] a charge on an upper surface of the insulating film (oxide layer 2); and determining [electrode pickup plate 12] the surface voltage of the insulating film (2) from the current, illuminating [via illumination source 16] the upper surface of the insulating film (2) during said measuring, and determining [see page 15] a band-bending voltage at an interface between the insulating film (2) and a substrate (not number but shown) as a difference between the surface voltage and a surface voltage of the insulating film (2) determined without said illuminating. Further, IBM teaches that the addition of using illumination source 16 to illuminate upper surface of the film and determining a band-bending voltage is advantageous because it provides for the real measurement of charges for all types of insulators in semiconductors and is independent of insulator thickness and integrity. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify

the apparatus of Verkuil et al by adding illumination source as taught by IBM in order to provide for the real measurement of charges for all types of insulators in semiconductors and is independent of insulator thickness and integrity.

Regarding claim 7, Verkuil et al disclose [see Fig. 1] a method for determining a surface voltage of an insulating film (oxide 12) comprising: depositing [via corona gun 18] a charge on an upper surface of the insulating film (12) [see also Abstract]; measuring [apparatus 10] a current to the wafer (15) during said depositing; and determining [Kelvin probe 20] the surface voltage of the insulating film (12) from the current. However, they do not disclose illuminating an upper surface of an insulating film as claimed. IBM disclose depositing [via charging bias 11] a charge on an upper surface of the insulating film (oxide layer 2); and determining [electrode pickup plate 12] the surface voltage of the insulating film (2) from the current, illuminating [via illumination source 16] the upper surface of the insulating film (2) with an alternating current modulated light source [shown inside light pipe 17] during said depositing. Further, IBM teaches that the addition of using illumination source 16 to illuminate upper surface of the film is advantageous because it provides for the real measurement of charges for all types of insulators in semiconductors and is independent of insulator thickness and integrity. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Verkuil et al by adding illumination source as taught by IBM in order to provide for the real measurement of charges for all types of insulators in semiconductors and is independent of insulator thickness and integrity.

Conclusion

Response to Arguments

The applicant's argue: " The cited art does not teach determining a surface voltage of an insulating film from a current to a wafer measured during deposition of a charge on an upper surface of the insulating film. Independent claim 1 recites in part: "depositing a charge on an upper surface of the insulating film; measuring a current to the wafer during said depositing; and determining the surface voltage of the insulating film from the current." Independent claims 14 and 19 recite similar limitations."

In response to the above arguments, the examiner disagrees and believes that the cited art does teach determining a surface voltage of an insulating film (oxide). In the cited art, col. 3, lines 23-43, it states: "The oxide current I.sub.OX may be expressed as the product of the oxide capacitance per unit area C.sub.OX and the derivative with respect to time of the voltage across the oxide (dV.sub.OX /dt). C.sub.OX can be calculated from E.sub.O.cndot.E.sub.OX /T.sub.OX. Where E.sub.O is the permitivity of free space, 8.86E-14 farads/cm, E.sub.OX is the relative dielectric constant of the oxide (3.9 for thermal oxide), T.sub.OX is the thickness of the oxide in centimeters. The derivative of V.sub.OX can be approximated by the change in V.sub.OX, .DELTA.V.sub.OX during a time .DELTA.t in seconds. An increment of charge as determined by the current integrator 26 is deposited on the oxide surface by the corona gun 18 and the voltage V.sub.OX measured by the Kelvin probe 20. After a delay, .DELTA.t, V.sub.OX is measured again. This then gives a value for dV.sub.OX /dt which is used to determine I.sub.OX. This change in voltage results from the reduction of charge over the interval .DELTA.t. The time .DELTA.t used varies with the oxide thickness and is picked to provide the desired sensitivity for measuring the oxide current. The increments of charge can also be summed to provide the cumulative deposited charge Q.sub.OX." Base on the above portion of the cited art the examiner believes the cited does teach determining a surface voltage of an insulating film (oxide).

6. Claims 3-4, 9, 11-12, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 3, the primary reason for the allowance of the claim is due a method for determining a surface voltage of an insulating film comprising detecting the charge on a reference sensor during said depositing and measuring a bias voltage of the reference sensor, wherein the surface voltage is approximately equal to the bias voltage of the reference sensor when the current to the reference sensor is approximately equal to the current to the wafer.

Regarding claim 4, the primary reason for the allowance of the claim is due a method for determining a surface voltage of an insulating film comprising depositing the charge until the current to the wafer is substantially constant, wherein the substantially constant current is approximately equal to a leakage current of the insulating film.

Regarding claim 9, the primary reason for the allowance of the claim is due a method for determining a surface voltage of an insulating film comprising depositing comprises exposing the wafer to a plasma.

Regarding claim 11-12, the primary reason for the allowance of the claim is due a method for determining a surface voltage of an insulating film comprising determining a parameter representing an electrical property of the insulating film from the surface voltage and altering a parameter of a process tool in response to the electrical property using a feedback or feed forward control technique.

Regarding claim 16, the primary reason for the allowance of the claim is due a method for determining a surface voltage of an insulating film comprising measuring the first current while altering a control voltage, and wherein said determining the first surface voltage comprises

determining a current turn-on point from the first current vs. the control voltage, and determining the first surface voltage from the value of the first current at the current turn-on point.

Since the examiner has not change art in the Office Action, the following is being applied.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
August 22, 2005